ABSTRACT OF THE DISCLOSURE

An integrated circuit includes a heterojunction thyristor device having an anode terminal, a cathode terminal, a first injector terminal operably coupled to a first quantum well channel disposed between the anode terminal and the cathode terminal, and a second injector terminal operably coupled to a second quantum well channel disposed between the anode terminal and the cathode terminal. Bias elements operate the heterojunction thyristor device in a mode that provides substantially linear voltage gain for electrical signals supplied to at least one of the first and second injector terminals for output to at least one output node. Preferably, the bias elements include a first DC current source operably coupled to an n-type modulation doped quantum well structure, a second DC current source operably coupled to a p-type modulation doped quantum well structure, a first bias resistance operably coupled between a high voltage supply and the anode terminal, and a second bias resistance operably coupled between the cathode terminal and a low voltage supply. The bias elements provide a current passing from the anode terminal to the cathode terminal that is below a characteristic hold current for the heterojunction thyristor device to thereby inhibit switching of the heterojunction thyristor device. The DC current provided by the DC current sources controls the amount of voltage gain provided by the heterojunction thyristor device.